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# Optimal double sided gate control of IGBT for lower turn-off loss and surge voltage suppression

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## Summary

The current density of power semiconductor devices continues to increase and, carrier injection has been enhanced by several methods even though turn-off loss tends to be increased. In order to address this problem, we propose a double sided gate IGBT and optimal gate control method for lower turn-off loss. TCAD simulation numerically shows that the proposed IGBT successfully decreases turn-off loss. Furthermore, the turn-off loss is further decreased with optimal control of the double sided gate without surge voltage increase. In addition, we consider the effects of stray inductance on the performance of double sided gate IGBT.

## 1 Introduction

Insulated Gate Bipolar Transistors (IGBTs) have been widely applied for various fields and products, such as home appliances, electric vehicles and renewable energy systems. Therefore, IGBTs have improved performance for expanding the applied range and demand. In particular, the increase of rated current density is a strong demand that has been realized for more than 25 years with several methods (see Fig. 1) [1]. In the future, it is expected to increase further according to the increased current density for realizing high power density of power electronics systems. However, further increase of rated current density needs a breakthrough because turn-off loss is increased by enhanced stored carrier for higher current density.

Thus, we propose a double sided gate IGBT [2-6]. This device is able to reduce turn-off loss dramatically by using two gates. Furthermore, we analysed optimal double sided gate control to optimize dynamic carrier distribution during turn-off by TCAD simulation to maintain low turn-off loss and surge voltage suppression [7-9].

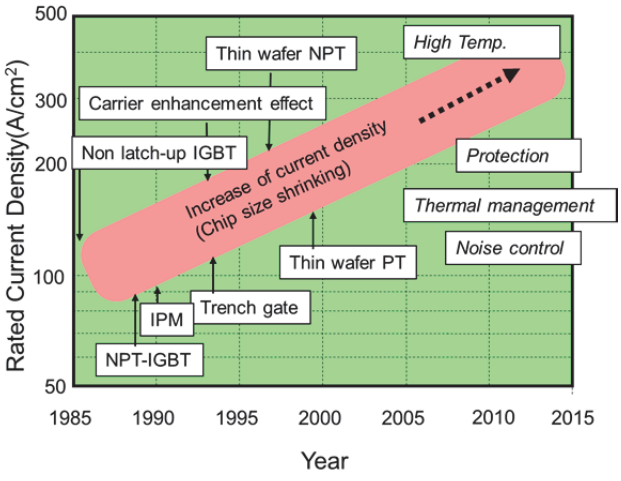
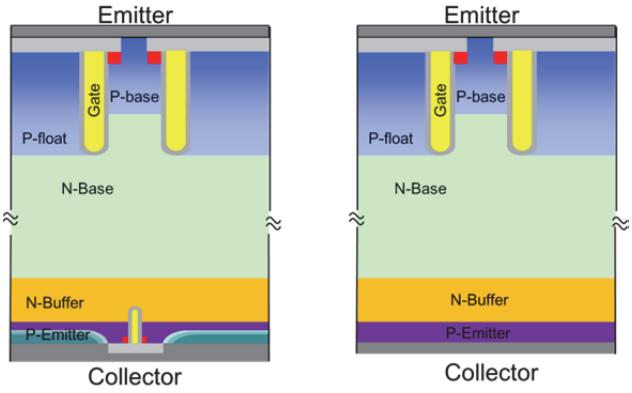



**Figure 1** Evolution of IGBT technology over the last twenty years [1]




(a) Double sided gate (b) Conventional structure

**Figure 2** Proposed and conventional IGBT structure

## 2 Turn-off loss reduction with double sided gate IGBT

### 2.1 Static performance of double sided gate IGBT

1200 V IGBT with a double sided gate has each gate at the emitter side gate (Gate 1) and the collector side gate (Gate 2) (see Fig. 2). This device is able to change the hole injection efficiency (γ) depending on Gate 2 voltage ($V_{G2}$).

Hole injection efficiency decreases from a maximum of 0.3 at 0 V to 0 over 5.5 V with an increase of Gate 2 voltage (see Fig. 3). The stored carrier also decreases from the collector side by reduction of hole injection with the increase of Gate 2 and eventually the hole is not injected like power MOSFET, because the hole injection is reduced due to lower resistance or a short-circuit between the collector electrode and the N-Buffer via the N-Chanel along the trench structure of Gate 2.

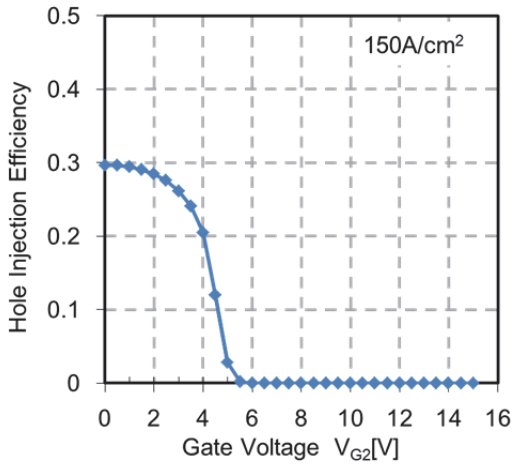



**Figure 3** Relationship between hole injection efficiency and gate voltage

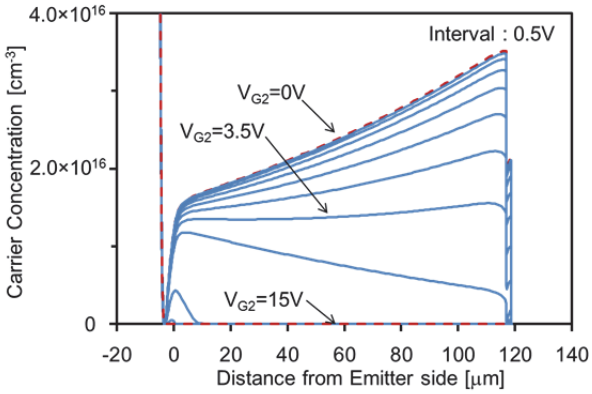


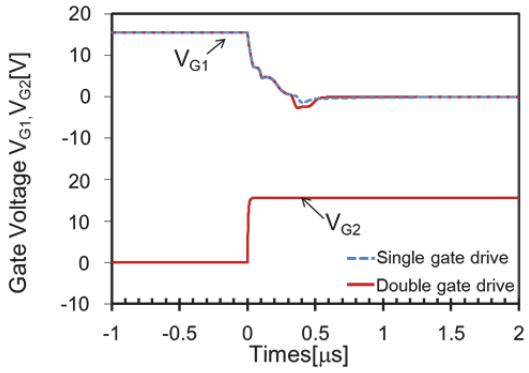

**Figure 4** Carrier distributions at each collector side gate voltage

## 2.2 Turn-off loss reduction by control of hole injection efficiency during turn-off

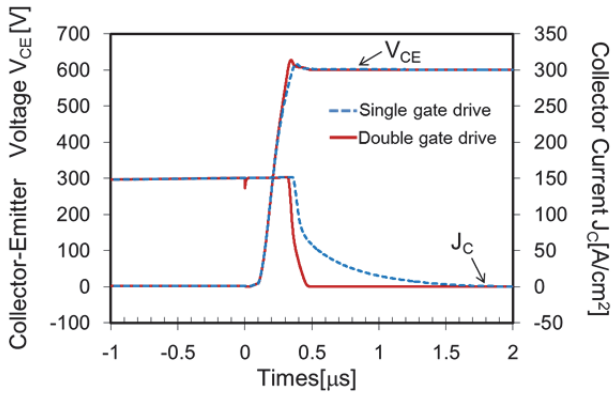
It is expected that turn-off loss is reduced by Gate 2 because it can instantaneously decline hole injection and eventually reduce stored carrier during turn-off. We simulate turn-off at each method of double gate drive and single gate drive assuming the conventional structure. The double gate drive is at the same timing of turn-off of Gate 1 and turn-on of Gate 2.

The Gate 1 voltage ($V_{G1}$) of both of double and single gate drive is almost the same as shown in Fig. 5. The double gate drive is able to reduce the tail current significantly by turn-on of Gate 2. In the case of single gate drive, hole injection efficiency basically increases and finally reaches 1 during turn-off. In the case of double gate drive, hole injection efficiency begins to decrease at turn-on of Gate 2 and the carrier is not injected from the collector side. As a result, the stored carrier is swept out fast and it can reduce the tail current significantly.

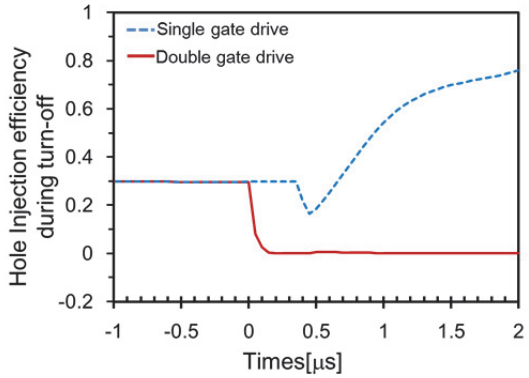
Eventually, the trade-off between saturation voltage and turn-off loss improves about half of the turn-off loss for wide $V_{CE(sat)}$ range (see Fig. 6). In the case of high current density of 300 A/cm$^2$, trade-off loss is also decreased to a half.




(a) Gate voltage




(b) Collector voltage and current




(c) Hole injection efficiency during turn-off

**Figure 5** Turn-off waveforms of double gate drive and single gate drive (Conventional drive method)

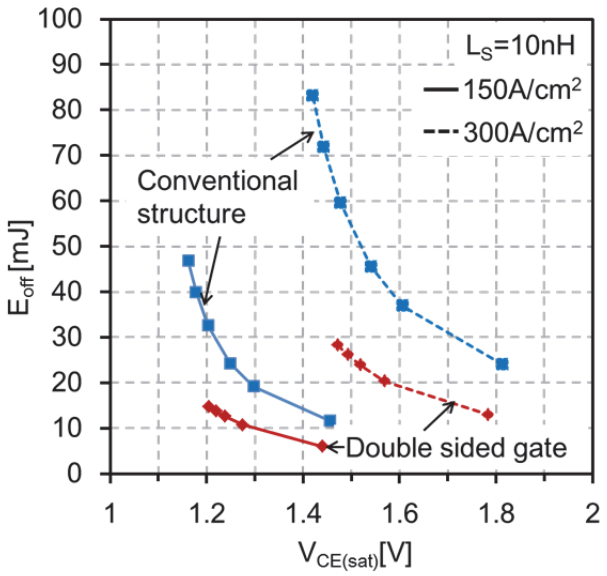
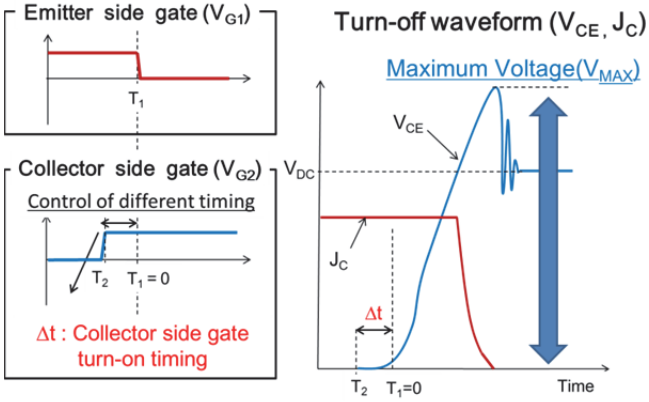



**Figure 6** Trade off curve for double sided gate IGBT and conventional IGBT

## 3 Optimal gate control of lower loss and surge voltage suppression

When Gate 2 is turned on earlier than turn-off of Gate 1, further turn-off loss reduction is expected because carrier injection is declined before turn-off of Gate 1. However, fast turn-off by a few stored carriers triggers a large surge in voltage. Therefore, we analyzed the relationship between turn-off loss with maximum surge voltage and the timing of the gate control. The schematic waveform and definition of the timing are shown in Fig. 7. We defined the time of turn-off of Gate 1($T_1$) as 0, and the time difference of turn-on of Gate 2 ($T_2$) as Δt.




(a) Gate voltage (b) collector voltage and current

**Figure 7** Schematic waveform and analysis method with definitions

In the case of Δt > 1.0 μs, the turn-off loss ($E_{off}$) is the largest and the maximum voltage ($V_{max}$) is the lowest. The values are the same as the conventional IGBT (see Fig. 8).

In the case of -0.1 μs < Δt < 0.9 μs, the $E_{off}$ is lower and $V_{max}$ is the lowest.

In the case of -0.8 μs < Δt < -0.2 μs, the $E_{off}$ indicates the lowest at Δt = -0.6 μs though large $V_{max}$ occurs.

In the case of Δt < -1.0 μs, the stored carrier is removed before turn-off of Gate 1 and large loss occurs. At a result, optimal control of Gate 2 is considered to be Δt = -0.1 μs. The $E_{off}$ is reduced to 80 % of the same timing of Gate 1 and Gate 2 as shown in Fig. 9.

When turn-on of Gate 2 is in the range of -0.8 μs < Δt < -0.2 μs, carrier is suddenly swept out before turn-off of IGBT (see Fig. 10). Therefore, a significant surge in voltage occurs. The required distance between the pn junction and the final removal point of the stored carrier (D) for surge voltage suppression is analytically indicated in the following equation.

$$D > \frac{2 \cdot V_{DC}}{E_{crit}}$$

Where $V_{DC}$ and $E_{crit}$ is supplied DC voltage and critical electric field for avalanche respectively. We used the following assumption for making the equation.

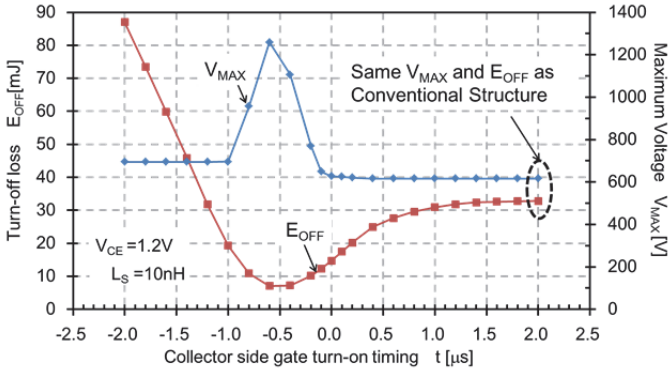



**Figure 8** Dependence of turn-off loss and maximum voltage at time interval

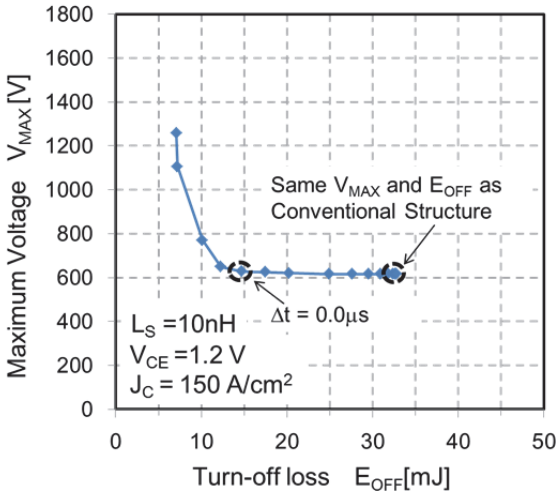



**Figure 9** Trade off curve between $E_{off}$ and $V_{max}$ for 10 nH

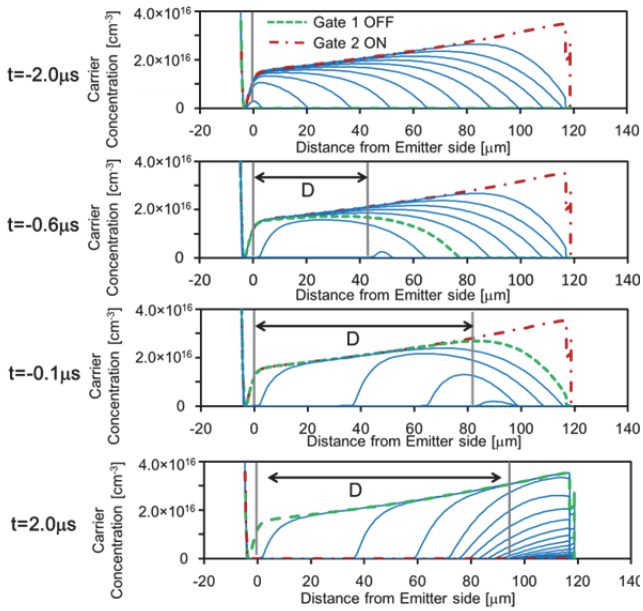



**Figure 10** Carrier profile during turn-off of IGBT (time interval of 0.1 μs with finally remaining carrier profile)

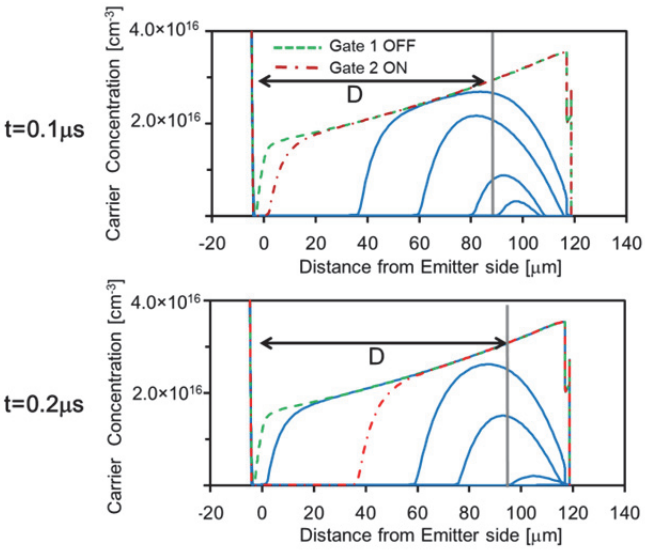



**Figure 12** Carrier profile during turn-off of IGBT at 100 nH (time interval of 0.1 μs with finally remaining carrier profile)

・Applied voltage to IGBT is determined only to triangular electric field on emitter side because triangular electric field on collector side is lower.

・Maximum electric filed is determined by critical electric field for avalanche

Result of the calculation using $2x10^5$ V/cm for $E_{cirt}$ and 600 V for $V_{DC}$, D is 60 μm in this simulation condition.

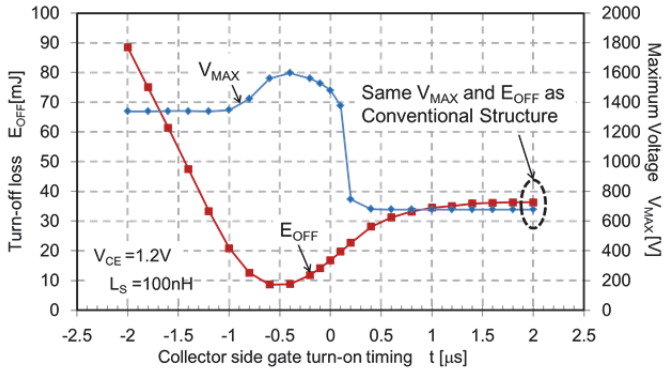



**Figure 11** Dependence of turn-off loss and maximum voltage at time interval (100 nH)

We considered the optimal control of double sided gate IGBT with changing stray inductance ($L_S$). We simulated turn-off waveform at $L_S$ = 100 nH. It indicates that $E_{off}$ increases and $V_{max}$ is higher by the effect of high stray inductance as shown in Fig. 11. Optimal timing of Gate 2 for surge voltage suppression changes at each stray inductance. Optimal control of Gate 2 is considered to Δt = -0.1 μs to turn-off of Gate 1 at 10 nH. In the case of 100 nH, it is considered to Δt = 0.2 μs to turn-off of Gate 1.

Not only the timing, the lowest $E_{off}$ is larger by large stray inductance because large D is required for maximum voltage supresssion with remained stored carreir at the collector side (see Figs. 12 and 13). Thus, low stray inductance in the circuit is required to maximise the effect of the double sided gate IGBT

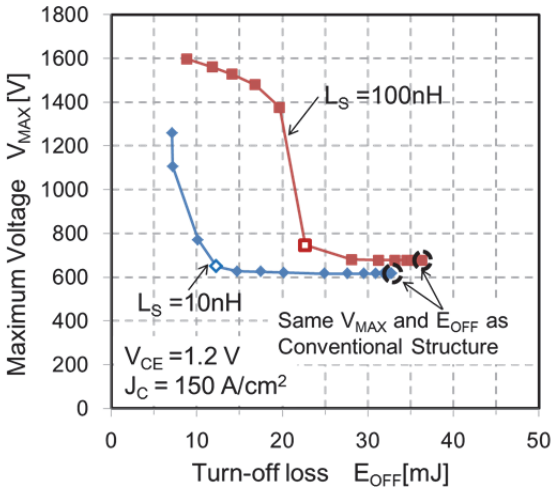



**Figure 13** Trade off curve between $E_{off}$ and $V_{max}$ for 10 nH and 100 nH

# 4 Conclusion

We proposed an IGBT with a double sided gate and an optimal control method. This device significantly reduces turn-off loss by dynamic hole injection control with the collector side gate. Furthermore, we proposed an optimal control method for further low turn-off loss. Low stray inductance of circuit is required to maximize the effect of the double sided gate IGBT.

# 5 References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